division. Gunn devices operating as frequency dividers can be used for this purpose [8]. In case of a parallel-series conversion the output signals of the ECL circuits must be sharpened by similar gate circuits. Pulse stretching is not necessary.

Conclusion

Monolithic circuit integration on GaAs can be used to an advantage in a multiplexing technique in the subnanosecond range. Planar Gunn devices, which due to their complex performance make possible a variety of logic functions, are employed as active components. A shift register is described which performs the logic AND operation and the pulse delay in one Gunn device per stage. The pulse delay is realized as the transit time of a domain in the channel of the Gunn device. A shift register was fabricated, the Gunn devices of which act as delay sections of about 25 μm. First experimental results prove the suitability of the circuit for multiplexing and demultiplexing operation at approximately 1.9 Gbit/s. Provided that the dimensions of the circuit are decreased, it can be expected that some gigabits per second can be processed.

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Diode Circuits for Pulse Regeneration and Multiplexing at Ultrahigh Bit Rates

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Abstract—**Clocked step-recovery diode (SRD) circuits are investigated for regenerating and multiplexing PCM-type signals in the range from 0.1 to a few gigabits per second. One regenerator type is particularly suited for operating with signals in the 1-V range, whereas a differential version employing a magic T was developed for handling signals of down to about 5 mV. By making use of line transformers as coupling networks, high-level versions have been cascaded. Experiments performed at 0.3 and 1 Gbit/s yielded voltage amplifications (peak amplitudes) of 2.5–5.5 for single stages, and insertion power gains of 7–11 dB for 2–3 stage cascades. Diode stages have also been used for multiplexing 4 and 2 individual bit streams to give a combined output signal at 1 and 2 Gbit/s, respectively. In a preliminary multiplexer experiment an output at 4.5 Gbit/s was obtained. Finally, possibilities are discussed for improving the performance of the regenerators/multiplexers and for their applications.**

Manuscript received May 17, 1976; revised July 26, 1976. This work was supported by the Deutsche Forschungsgemeinschaft.
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I. Introduction

INTEREST IN PCM signals of ultrahigh bit rates (UHB), i.e., extending from about 0.1 to a few gigabits per second, has recently grown, among other things because of the impressive bandwidth potentialities offered by communication systems of the circular waveguide and the laser/fiber-optic types. Here we describe investigations on clocked diode circuits which might be suited for regenerating and multiplexing PCM pulse signals within the range of these high bit rates.

The circuit concepts under discussion are related to a diode pulse amplifier which was proposed more than 20 years ago [1] but which received only limited attention [2]–[5]. The amplifier relies essentially on the minority-carrier storage in the diffusion capacitance of a p-n diode and on the turnoff transient when the stored charge has been

removed by an applied reverse pumping current. A more detailed description of the operation is given in Section II.

It was proposed to use such circuits with modern fast step-recovery diodes (SRD's) as regenerators for PCM signals of high bit rates [6]. An experiment performed with a single stage at 250 Mbit/s showed that it was possible to simultaneously restore pulse amplitude (at reduced pulse-width), pulse edges, and phase (retiming) of PCM-type *RZ* signals [6]. In a further experiment several bit streams were combined by using clocked diode circuits of the type considered, with *RZ*-signal multiplexer action obtained up to 1 Gbit/s [7].

In this paper we first describe an improved diode-regenerator circuit for which a sine-wave clock suffices, giving results of experiments performed at 0.3 and 1 Gbit/s (Section II). To increase the obtainable gain, several stages were cascaded via suitably designed line transformers (Section III). In a second version, offering substantially increased sensitivity, the difference in impedance of two diodes is made to offset the previously balanced condition of a magic T (Section IV). Multiplexer stages were realized delivering output *RZ* pulse trains up to 2 Gbit/s, in preliminary results up to 4.5 Gbit/s (Section V). Finally, we will give an outlook on the prospects and possible applications of the investigated circuits (Section VI).

II. Diode Regenerator (Single Stage)

Fig. 1(a) shows a schematic diagram of a modified pulse regenerator stage here investigated which contains *two* SRD's, one Schottky-barrier diode (SD), and a resistive load R_L. A signal generator, delivering an input pulse voltage $v_S(t)$, and a *sinusoidal* pump (clock) generator of voltage $v_P(t)$ are connected to the circuit. The operation cycle of the regenerator consists of 1) a charging phase during which an applied input pulse injects charge into SRD_1 (carrier storage), and 2) a subsequent discharging phase, characterized by the pump generator extracting the signal charge from SRD_1 and driving a current through the load R_L. Because of appropriately adjusted bias voltages and the negative sine half-wave of the pump during phase 1), the diodes SD and SRD_1 are then slightly forward biased, and SRD_2 takes up charge from the pump. The diffusion capacitance of SRD_1 can be charged by the input signal via the low-impedance path provided in this way—"low" in relation to the comparatively high load resistance. At the same time, a similar amount of charge is subtracted from the precharge in SRD_2. The temporal response of the charges in the two SRD's is schematically indicated in Fig. 1(b), related to the input, pump, and output signals.

When the input pulse has ended and phase 2) starts, the then existing positive sine half-wave of the pump voltage first discharges SRD_2, and subsequently also the diode SRD_1 via the load R_L, as soon as SRD_2 has switched from a low-impedance to the high-impedance state. In this way an output pulse is obtained across the load resistor, the leading pulse edge being formed by SRD_2 and the trailing edge by SRD_1. For possibly occurring zero-bit

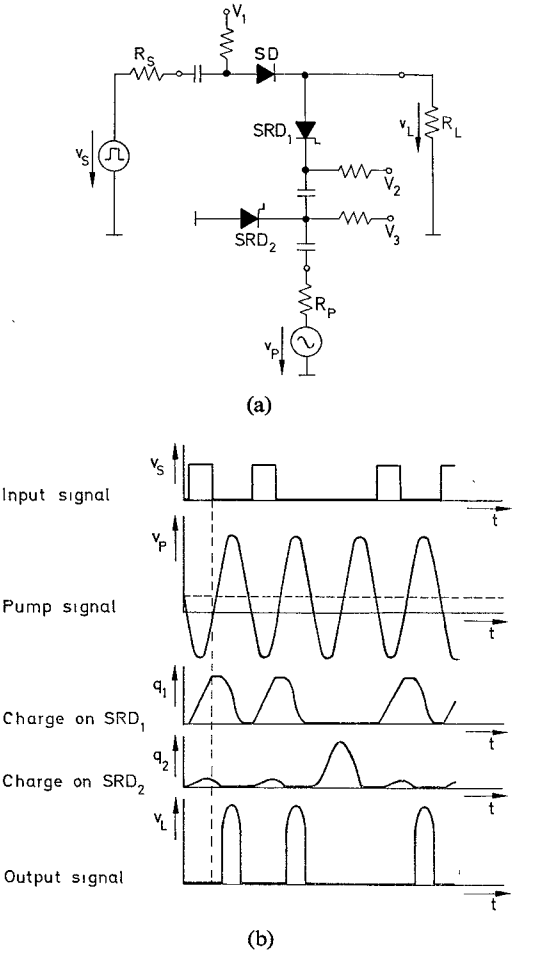

Fig. 1. Basic circuit (a) and ideal pulse response (b) of diode regenerator.

input signals (*no* input pulse) SRD_1 remains practically without diffusion charge. On the other hand, a continuous pulse train is obtained at the output if a forward dc current is applied to the input (at terminal V_1). This follows from the fact that the regenerator responds to the time integral of the injected current (i.e., charge) over the interval between two successive discharging phases, delivering the same value of charge to the load in case we neglect losses (caused, e.g., by carrier recombination in SRD_1). Because of this integrating feature, the circuit has the property of removing time jitter which an input pulse signal may exhibit, and shows no response to input baseline ripple as long as it equals zero over the charging interval. Proper operation in this way obviously requires a fixed (180°) phase shift between the input pulse train and the pump signal [see Fig. 1(b)]. In the experiments described as follows, the pump was locked directly to the input-signal generator while in actual system applications of regenerators (repeaters) phase-locked loop techniques are generally used for deriving the clock phase from the signal.

A single stage can provide a certain amount of voltage and current amplification as well as power gain. In the special case of equal charging and discharging currents

TABLE I
DATA OF DIODES USED

Diode	Used for	$C_{J,0V}$/pF	V_{br}/V	τ_{eff}/ns *	t_t/ps *	R_{ser}/Ω	Type, Case, Manufacturer
SRD	Figs. 8, 9, 10	0.8	20	15	50		Si-pin, A4S008, LID (Aertech)
	Figs. 2, 3,6, 11 (SRD_2)	0.5 to 0.7	20	15	50		Si-pin, A4S386, LID (Aertech)
	Fig. 5 (SRD_2)	1.8	42				Si-pin, 15CA2, micropill (Siemens)
	Figs. 2, 6, 11 (SRD_1)	0.45			50		Si-pin, developmental, LID (Siemens)
SD	Figs. 5, 3	1.6	70			25	Si, 5082 - 2844, LID (HP)
	Figs. 11, 2, 6 (1st stage)	0.8	5			> 7	Si, A2S031, LID (Aertech)
	Fig. 6 (2nd stage)	0.3	8			3	GaAs, 1SS11, micropill (NEC)
		0.13	3			7 to 8	Si, EH 320, LID (Thomson CSF)

* measured in standard test circuit according to manufacturer's specifications

through SRD_1, giving approximately equal input and output pulsewidths, the power gain is given, to first order, by the square of the ratio between output impedance and input impedance. Since, however, the discharging pump current can be chosen to be substantially higher than the charging current, peak output currents and voltages higher than those at the input can be obtained (though at the expense of smaller pulsewidth). The current-integrating response of the amplifier leads mainly to a broadening of the output pulse if the amplitude of the input pulse is increased at constant pump current, and primarily to a rise in output pulse height with growing pump amplitude at constant input level (with an upper limit on pump amplitude set in our experiments by the reverse breakdown voltage of SD).

The low-frequency limit of the regenerator lies between 50 and 100 Mbit/s because of effective minority-carrier life times of τ_{eff} = 10–20 ns which the employed SRD's exhibited (see Section V). For longer intervals the injected charge cannot be stored. The high-frequency limit is ultimately caused by the SRD turnoff time of 30–100 ps, but the *RC* time constant of the output circuit and other effects show, in practice, a more severe influence.

Fig. 2 gives a typical experimental result (diode data in Table I) obtained at 1 Gbit/s with a hybrid-integrated thin-film stage according to Fig. 1(a), indicating a voltage "amplification" of $a_v \approx 2.6$ across $R_L = 100\ \Omega$. Voltage (current) amplification is here and in the following defined as the ratio of the voltage (current) difference between minimum 1-bit pulse height and maximum baseline ripple excursion at the output to the corresponding voltage

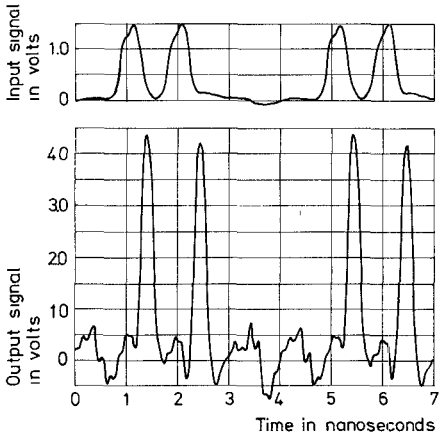

Fig. 2. Measured pulse response of diode regenerator; single stage (1 Gbit/s), $R_L = 100\ \Omega$, $R_{ref} = 50\ \Omega$.

(current) difference of the input signal. It is important to point out that, as stated previously, a large height of the output pulse generally goes along with a corresponding reduction in pulsewidth. A remark on measured current amplification and power insertion gain will be made in Section III. The displayed "input signal" is the pulse train obtained across an ohmic reference resistor R_{ref} (of the value specified) connected directly to the signal generator. In an experiment at 0.3 Gbit/s, which revealed less baseline ripple, we obtained $a_v \approx 3.2$.

The operation of slightly altered diode circuits [8], with primarily an SD used instead of SRD_2 and the sine-wave pump replaced by a pulse source, was simulated on a

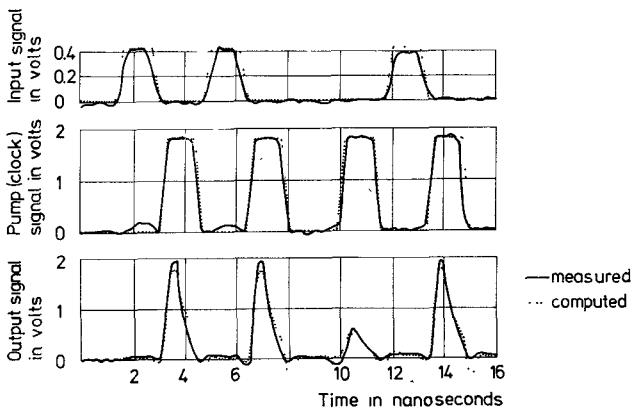

Fig. 3. Computed and measured pulse responses of diode regenerator (with pump pulse source); single stage (0.3 Gbit/s), $R_L = 150\ \Omega$, $R_{ref} = 50\ \Omega$.

digital computer using a modified version of the network analysis program REGENT [9]. The circuit alteration has mainly the effect that the leading edge of the output pulse is now being formed by the leading pump-signal edge. In the program the SD's were modeled by an equivalent circuit comprising a bulk resistance, a voltage-dependent forward conductance, and an averaged constant junction capacitance. For the SRD this circuit was extended by a voltage dependent diffusion capacitance, and an appropriate voltage dependence of the junction capacitance was introduced. Case inductance and capacitance were neglected. Fig. 3 shows both a result which was typical for the simulations, as well as the corresponding pulse trains measured on the realized amplifier. Simulation and measurement agree essentially, each of them showing, for example, the occurrence of a spurious pulse at the 0-bit site. These 0-bit pulses (see also Figs. 2, 5, 6) are caused by some unwanted charge occurring in SRD_1 due to a small bias and particularly by the junction capacitance C_j. Presently, we are carrying out a more sophisticated modeling and investigation of SRD devices in order to further improve the computer simulation and to obtain data for the design of optimum diodes, see e.g., [10].

III. Regenerator Cascade

As described previously, the regenerator circuit responds to charge, but the amount of *charge* transferred to the output at best only equals that received at the input. For achieving a substantial power gain several stages must, therefore, be cascaded by inserting a coupling network between them which increases the charge (input current) from stage to stage. As a possible solution this network can be formed by a step-down transformer, the output impedance of which should match the averaged input impedance of the succeeding stage.

We have performed experiments at 0.3 and 1 Gbit/s employing transmission-line transformers (e.g., [11]) of particularly large bandwidth. The transformers developed for this purpose were either of the twisted-pair line (100 Ω:25 Ω), or of the stripline [12] (160 Ω:50 Ω; 50 Ω:14.5 Ω), types (see Fig. 4). Characteristic of line transformers is the

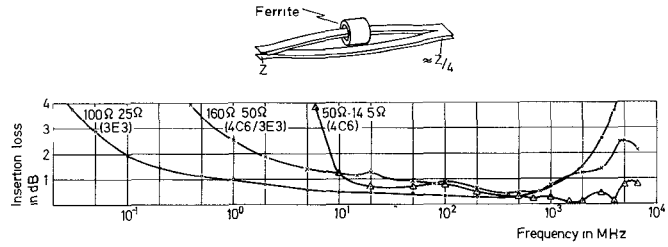

Fig. 4. Measured performance of line transformers.

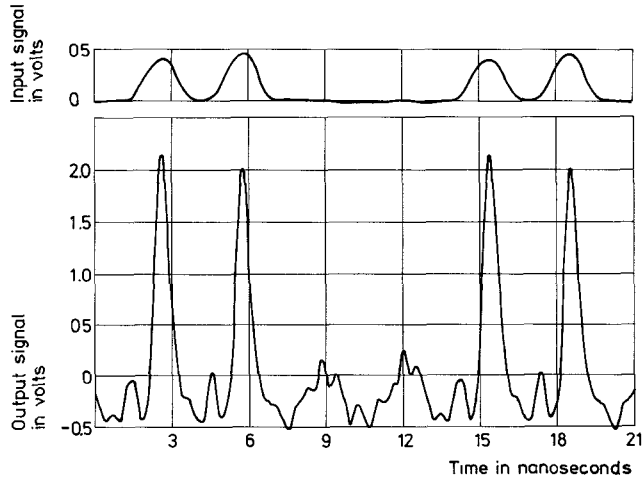

Fig. 5. Measured pulse response of diode regenerator; 3-stage cascade (0.3 Gbit/s), $R_L = R_{ref} = 25\ \Omega$.

series connection of the lines on one side, and shunting them on the other side. The short-circuit loop created in this way at the series side must be neutralized for good low-frequency performance by inserting suitable ferrite material. The measured performance of the transformers is given in Fig. 4. When the single regenerator stages of Section II were terminated by the transformers, they showed approximately a current amplification as to be expected from the corresponding transformation ratio.

A cascade consisting of three single stages after Fig. 1(a), coupled by 100/25 Ω transformers, showed a performance at 0.3 Gbit/s as reproduced in Fig. 5. The last stage was terminated by a transformer with a 25-Ω load across its output. The sine-wave pump signals, which were derived from a common source, had to be increased in amplitude from stage to stage and shifted in phase by 180° plus the phase shift of the corresponding transformer. With the 3-stage circuit, thought to be not yet fully optimized, an average-power insertion gain, between $R_{ref} = 25\ \Omega$ and $R_L = 25\ \Omega$, of about $g_{\bar{p},i} = 10$ dB was obtained. The overall *charge* amplification amounted to $\alpha \approx 2.4$ where the charge associated with the input current flowing through $R_{ref} \approx 25\ \Omega$ was taken as the reference input charge. The charge actually stored in SRD_1 of the first stage might have been somewhat smaller than that calculated from the purely resistive R_{ref} (because of the average input impedance probably being higher than 25 Ω), in which case the actual α is correspondingly larger. According to Fig. 5 the voltage amplification was about 4.5. Curves obtained with a 2-stage

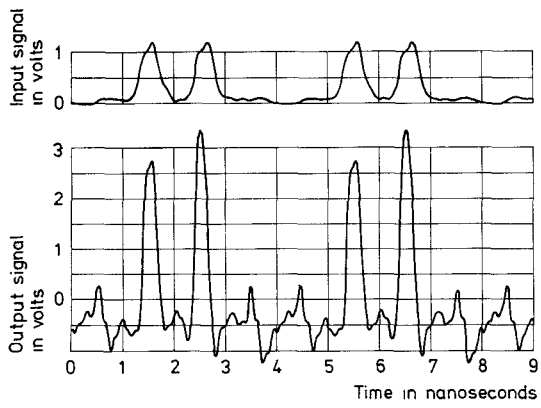

Fig. 6. Measured pulse response of diode regenerator; 2-stage cascade (1 Gbit/s), $R_L = R_{ref} = 25\ \Omega$.

1-Gbit/s version using, again, 100/25-Ω transformers are shown in Fig. 6. Here, a voltage amplification of 2.4, and $g_{\bar{p},i} \approx 7.4$ dB were measured. (Note the nearly three times higher input level; cf. Section VI.)

All output curves (apart from Fig. 3) exhibit a small pulse prior to the regenerated 1-bit signals. This results from part of the input signal reaching the output directly during the charging phase. As this part of the charge is not stored in SRD_1, it represents a loss. Further losses are caused by the passband attenuation of the transformers, mismatches, carrier recombination losses, discharging of the diffusion capacitance via the external circuit, and by some pump current leaking off to the preceding stage via the junction capacitance of the reverse-biased SD. The latter effect is thought to be responsible also for the unequal height of the output pulses.

IV. Differential Circuit

The circuits described so far are not suited for regenerating weak pulses (some millivolts to 100-mV range). For low-amplitude applications a second type of regenerator—however, not limited to low-level operation—was developed, namely, a differential circuit incorporating an extremely broad-band magic T (180° hybrid) as shown in Fig. 7, [13]. In [14] the usefulness of a magic T together with two SRD's had already been reported for generating clean subnanosecond pulse trains of high repetition rate, but the application as a differential *amplifier* was not considered.

As shown in Fig. 7(a), two SRD's are connected to a pair of opposite ports (subscript S for "signal," R for "reference"), whereas a sine-wave pump generator (clock) and the load terminate the other pair of opposite ports. (Note SRD's being *shunted* across the ports.) The input signal is applied to SRD_S, and SRD_R is loaded by an impedance equaling that of the signal generator. For the experimental circuits special 6-port coaxial/stripline magic T's with a lumped branching point [15] [Fig. 7(b)], which avoid resonant structures and show good broad-band matching, were modified for this particular use. With the 6-port T the circuit was arranged to have two output ports, delivering practically identical signals (their polarity can be chosen at will), and two pump ports fed from the

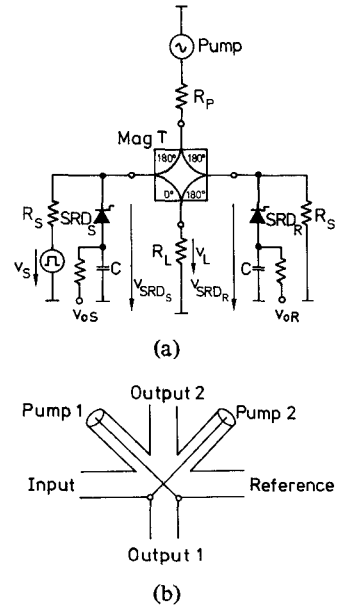

Fig. 7. Differential regenerator circuit (a) and schematic representation of the broad-band magic T (b).

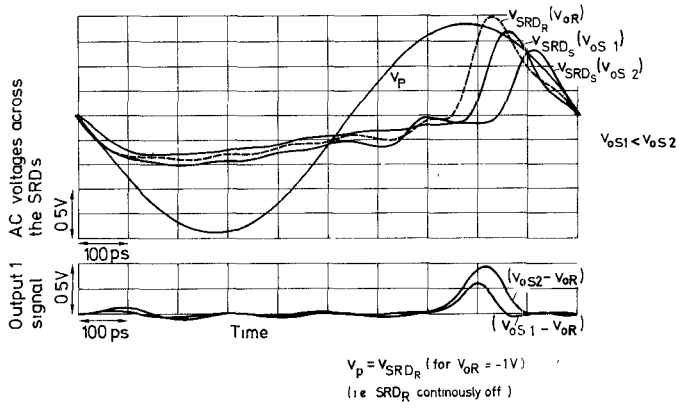

Fig. 8. Measured pulse behavior of differential regenerator to demonstrate operation principle.

same pump. The bandwidth of the 6-port T's ranged about from 100 kHz to 10 GHz. For the two SRD's matched pairs were used selected on the basis of their $C_j(V)$ curves.

The operation principle is as follows; refer to Figs. 7 and 8. The diodes are first supplied with the same basic charge by applying appropriate bias voltages and the charging pump half-wave. An input signal then causes a slight charge decrease in SRD_S (impedance of forward-biased diodes being small compared to 50-Ω input impedance of magic T). Therefore, during the subsequent discharging pump half-wave, SRD_S switches somewhat earlier from the low-impedance to the high-impedance state than does SRD_R. The switching process is illustrated in Fig. 8 for an excess of charge in SRD_S caused by differing bias ($V_{0S1} > V_{0S2} > V_{0R}$; no input signal). As long as the SRD impedances are unequal, the magic T is unbalanced, and energy is transferred from the pump to the load. In this way SRD_R forms mainly the leading edge, and SRD_S the trailing edge, of the generated output pulse (Fig. 8, bottom). After the switching

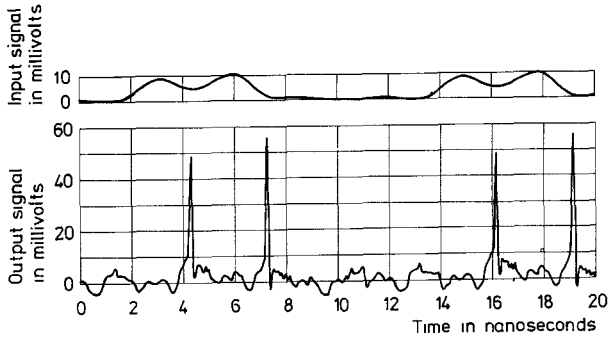

Fig. 9. Measured pulse response of differential regenerator; single stage (0.3 Gbit/s), $R_L = R_{ref} = 50\ \Omega$.

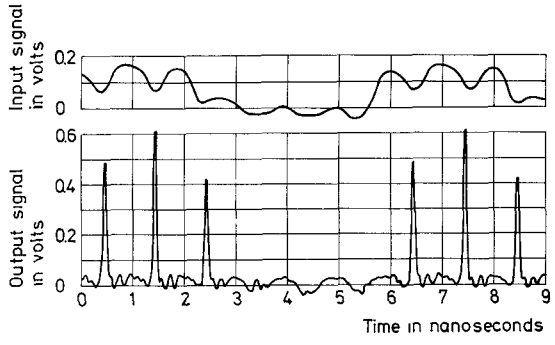

Fig. 10. Measured pulse response of differential regenerator; single stage (1 Gbit/s), $R_L = R_{ref} = 50\ \Omega$.

the diode voltages follow approximately the pump sine wave $v_p(t)$.

Fig. 9 shows typical pulse trains measured (across *one* output port) on a single stage at 0.3 Gbit/s and across a 50-Ω load. In this case $g_{\bar{p},i} \approx 6.4$ dB (sum of both output ports) and $a_v \approx 5.2$ were obtained. The (actual) power gain was probably higher than this value of insertion gain $g_{\bar{p},i}$ because the input impedance of the regenerator seemed to be smaller than 50 Ω. Operation was possible with input pulse amplitudes down to a few millivolts. At 1 Gbit/s the curves given in Fig. 10 were recorded, with the voltage amplification being 3.9 and $g_{\bar{p},i} \approx 4.2$ dB. The input signal, particularly in Fig. 10, shows a tendency towards an *NRZ* pattern; the inherent regenerator action turns this into a definite *RZ* signal at the output. In Figs. 9 and 10 the obtained output pulses show a greater height when relatively much charge was supplied during the corresponding input charging interval. The height of all pulses became practically equal for clean *RZ* input signals.

It is intended to also cascade differential stages. This will be best accomplished by connecting the *two* output ports, chosen to deliver signals of opposite polarity, via suitable impedance transformers to the SRD_S and the SRD_R ports, respectively, of the following stage. Use will thereby be made of the full output.

V. Multiplexers

Time multiplexing of n parallel bit streams to form an output signal having a rate which is n times higher can in a relatively simple way be achieved by employing n single

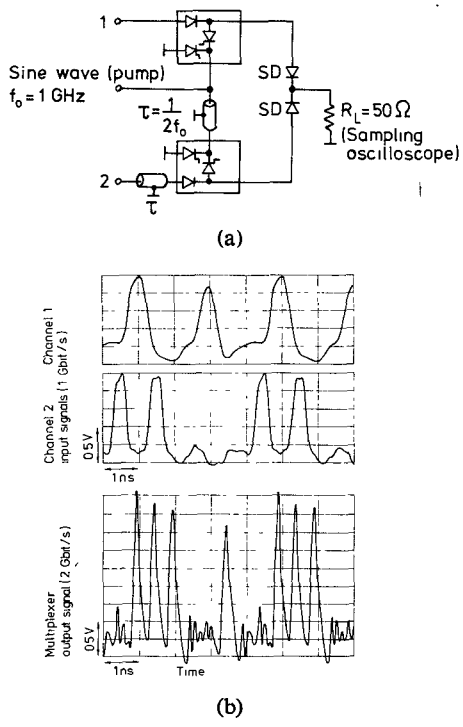

Fig. 11. Schematic diagram (a) of 2-channel 1-Gbit/s to 2-Gbit/s multiplexer, and measured performance (b).

diode regenerator circuits working into a common load [7]. Operation relies on the fact that the diode circuits are capable of delivering output signals which exhibit considerably smaller width and (possibly) greater height than the input pulses. Multiplexer operation in this way, by using circuits with a pulse pump source, was demonstrated to be feasible for pure *RZ* signals up to 1 Gbit/s at the output [7].

We have performed multiplexer experiments with circuits of the type shown in Fig. 1(a). The schematic diagram of the multiplexer circuit, in this case for combining two pulse streams into a 2-Gbit/s signal across a 50-Ω load, is given in Fig. 11(a). The result obtained when multiplexing two continuously repeated 4-bit word sequences into an 8-bit word train is shown in Fig. 11(b). Voltage amplification is seen to occur. Experiments have further been performed with four diode circuits, two of which received differing 0.25-Gbit/s signals while the other two were supplied with dc voltages. As necessary, the narrowing of the original 0.25 Gbit/s input pulses has been relatively still more pronounced, to provide the 1-Gbit/s output signal.

Figs. 9 and 10 have demonstrated that the differential stage yields particularly narrow output pulses. This suggests to investigate the use of such circuits for realizing multiplexers at even higher bit rates or with more input channels. In a preliminary experiment we have combined the two 1-Gbit/s signals (Fig. 10) as obtained from the (two) output ports of a single differential stage. Before feeding them into the common load, a time delay was introduced between the two signals such as to just *separate* the pulses belonging to the same input pulse. Spacing between two adjacent pulses has been 220 ps (corresponding to 4.5 Gbit/s). One

might thus expect to obtain multiplexer action using differential circuits at output bit rates up to several gigabits per second (for *RZ* operation).

Table I gives the most relevant data of the SRD's and SD's employed in the regenerator and multiplexer experiments, including junction capacitance C_j, reverse breakdown voltage V_{br}, effective minority-carrier life time τ_{eff}, turnoff time t_t, and series resistance R_{ser}.

VI. Conclusions

It has been shown that modified versions of the diode pulse amplifiers proposed already a considerable time ago [1] can be operated up to the gigabit-per-second range by employing modern semiconductor diodes and improved circuit design.

As an interesting feature, regenerator stages for PCM-type signals were able to provide voltage and current amplification, delivering pulses with amplitudes of up to some volts and with base widths of a few 100 ps. The upper limit on output amplitude (Fig. 6) was set by the breakdown voltage of the used SD. The circuits are also capable of simultaneously retiming the input signal. The property of narrowing the pulses can be favorably used for obtaining multiplexer action, with experiments performed up to 4.5 Gbit/s.

With a 2-stage cascade an average-power insertion gain of 7.4 dB was achieved at 1 Gbit/s, using broad-band line transformers to obtain the required charge increase. As a possible alternative for interconnecting individual stages, we intend to also investigate transistor coupling, in order to increase the obtainable power gain.

Improved performance depends, among other things, on advanced diode design (higher SD breakdown voltage → higher possible pump voltage; smaller SD and SRD junction capacitances → smaller leakage currents; lower series resistances → reduced energy loss; higher SRD "emitter efficiency" → reduced charge storage in contact layers; possibly: shorter SRD *i* layer → reduced turnoff time).

At higher bit rates a limiting factor is presented by the increased averaged SRD impedance during the pulse turnon part [16] preventing sufficient charge injection. With higher input-signal levels (cf. Fig. 6) this problem becomes less severe. Conditions are also more favorable in the differential circuit since there both SRD's carry a considerable precharge.

The circuit has the property of rejecting the dc component of the arriving input signal [see Fig. 1(a)]. This may lead to an unwanted precharge in SRD_1 depending on the bit pattern. It must be investigated how serious this effect will turn out to be in practical applications (with scrambled PCM signals and/or automatic bias control).

Applications of the investigated circuits may foremost be seen in the field of projected high-rate fiber-optic communication systems, i.e., in their electronic repeater, particularly for driving DHS laser diodes (low dynamic impedance!) or external modulators. The availability of high-current pulses at ultrahigh bit rates should make such applications possible. In a preliminary experiment a differential diode circuit was fed by an avalanche photodiode; it still has to be studied whether the narrow-width pulses thus obtained in the front-end stage can be further processed. Generally, the spike-type pulses from the differential regenerator are considered to be useful for triggering threshold-level devices.

Acknowledgment

The authors wish to thank Siemens AG and the Hewlett Packard Company for providing the diodes, and AEG-Telefunken for use of the original REGENT computer program. They also wish to thank H. U. Schreiber and H. J. Rosenhahn for their technological assistance.

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